REMARKS

Claims 4, 6, 8, 11, and 12 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. With respect to claim 4, the Examiner rejects the claim because the phrase "input parts" is not described in the specification. Applicant has amended the phrase "input parts" to be "input terminals." The present specification discloses, at page 8, lines17-19, data driver ICs 15-1 to 15-10 that have input terminals. Withdrawal of the rejection of claim 4 is respectfully requested.

Regarding claims 6, 8, and 12, the examiner asserts that the phrase "plurality of bits" is not described in the specification. In response, applicant asserts that the present specification discloses, at page 20, lines 16-23, that a dot is composed of 3 colors, and that each of the colors is specified using 8 bits. Accordingly, the specification does disclose that a dot is comprised of a plurality of bits. For this reason, withdrawal of the rejection of claims 6, 8, and 12 is requested.

Regarding claim 11, the examiner asserts that the phrase "same horizontal line" is not described in the specification. Accordingly, Applicant has removed this phrase from claim 11. Withdrawal of the § 112 rejection is respectfully requested.

Claim 11 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Go (U.S. Patent No. 6,320,566). Applicant traverses this rejection because Go fails to disclose (or suggest) that a timing controller displaces the phase between the data signals of the odd-number dots and even-number dots by 180 degrees.

Go discloses that a data driver IC 120 displaces the phase between first video signals S1', S3' and S5' of the odd data lines D1, D3, and D5 and second video signals S2', S4' and S6' of the even data lines D2, D4 and D6 by 180 degrees (see col. 6, lines 23-27, Figs. 10-12).

The first video signal S1' is generated by using the data signal S1 received from the controller IC 100 and the first clock signal FD1, and the second video signal S2' is generated by using the data signal S2 received from the controller IC 100 and the second clock signal FD2 (see col. 6, line 64 to col. 7, line 14 and Figs. 10-12). As shown in Fig. 11, the controller IC 100 does not displace the phase of data signals S1 and S2. Instead, the data driver IC 120 displaces the phase between the first and second video signals S1' and S2' by 180 degrees. Accordingly, Go fails to disclose a timing controller that displaces the phase between the data signals of the odd-number dots and even-number dots by 180 degrees. For this reason, Applicant respectfully requests withdrawal of the rejection of claim 11.

Claims 1 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Misawa et al. (U.S. Patent No. 5,616,936). Applicant traverses this rejection because Go and Misawa, taken alone or in combination, do not disclose or suggest a liquid crystal display device with first and second clock signal lines that are equipped in parallel and have load capacitances that are equal or substantially equal by equipping the load means.

The examiner cites Go as teaching that first and second signal lines FD1 and FD 2 are arranged in parallel, as shown in Figs. 10 and 12. However, the examiner

acknowledges that Go does not disclose two clock signal lines having substantially equal load capacitances, and instead relies on Misawa to teach this feature. Misawa teaches, at col. 12, lines 31-39, that a CL line 218 and a CL line 219 are twisted, crossing near their centers. This twisted shape causes the average distance between the CL lines 218, 219 and the video signal bus to be approximately equal. The approximately equivalent distance between the CL lines 218, 219 and the video signal bus causes the load capacitances of the CL lines to be approximately equal as well. Accordingly, the load capacitance on the CL line 218 is equal to or substantially equal to the load capacitance of the CL line 219 only when the CL line 218 and the CL line 219 are twisted. Put another way, if CL line 218 and CL line 219 were arranged in parallel, the load capacitances would no longer be substantially equal. Accordingly, Go and Misawa, even when combined, do not disclose or suggest first and second clock signal wires that are both equipped in parallel and have load capacities that are equal or substantially equal by equipping the load means. Because the cited references fail to disclose or suggest this combination of features, withdrawal of the rejection of independent claim1 and its associated dependent claims is respectfully requested.

Additionally, an embodiment of the invention as recited in claim 1teaches that even if the load capacitances of the first and second signal lines that are arranged in parallel differ from each other, it is possible to adjust the load capacitances by the load means so as to have load capacitances that are equal or substantially equal (see p. 16, lns. 13 *et seq.* and Fig. 10). Go and Misawa also fail to disclose or suggest this feature of the present invention. Accordingly, Applicant again requests withdrawal of the rejection of claims 1 and 5.

Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Jeon et al. (U.S. Patent No. 6,690,347). Applicant traverses this rejection because Go and Jeon, taken alone or in combination, fail to disclose or suggest a selection signal that is used to select the first or second clock signal.

The present invention shows, in Fig. 18, that a driver circuit receives as input signals two clock signals CLK and /CLK, and a selection signal SL. These inputs are connected to a logic circuit so that signal CLK is used as the internal clock I-CLK if signal SL is high, and signal /CLK is use as the internal clock if signal SL is low. Accordingly, the selection signal is used to determine which clock signal is to be used within the driver.

The examiner recognizes that Go is silent regarding a selection signal, and relies on Jeon to teach a selection signal that is the basis for selecting either a first or second clock signal. However, Jeon merely discloses, at col. 10, lines 35-53, that a selection start signal is used to enable blocks of data lines. Jeon discloses using a shift register to produce the selection start signals. Odd-numbered stages of the shift register receive clock signal CLKH as an input, and even-numbered stages of the register receive clock signal CLKHB as an input. The output of each stage of the shift register is connected to a corresponding block of data lines as a selection start signal. When an output is high, the corresponding block of data lines is enabled. However, Jeon is silent regarding using the selection start signal as the basis for selecting either a first or second clock signal. Because Go and Jeon, taken alone or in combination do not disclose or suggest a selection signal, where the first or second clock

signal is selected based on the selection signal, withdrawal of the rejection of claim 7 is respectfully requested.

Claims 9 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Jeong (U.S. Patent No. 6,335,721). Applicant traverses this rejection for the reasons below.

Regarding claim 9, applicant traverses the rejection because Go and Jeong, taken alone or in combination, do not disclose a sampling memory that samples and stores data signals as defined in amended claim 9.

In the present invention, as shown in Fig. 12, the output of a first latch and a second latch is input into a sampling memory before being converted to an analog signal and output. The sampling memory alternately samples and stores the data signals received from the first and second latches.

The data driver IC (integrated circuit) shown in Go does not include a memory. As shown in Fig. 12, the data driver IC includes only a latch 200 and a set of XOR (exclusive OR) gates 210. The latch used in the driver IC of Go provides 6 outputs d1-d6, which are input into respective XOR gates 210. XOR gates receiving an odd output of the latch (d1, d3, or d5) also receive clock signal FD1 as an input. Similarly, XOR gates receiving an even output of the latch (d2, d4, or d6) receive clock signal FD2 as an input. The output of each of the XOR gates is applied to the data lines. However, Go is silent regarding any memory within the data driver IC.

Similarly, Jeong does not disclose or suggest a driver equipped with a memory. Fig. 4 of Jeong shows a source driver that includes a shift register 200. The outputs of the shift register are input into a latch block 300. The outputs of the latch block are provided to a level shifter 400, which generates negative and positive polarity video signals. Those signals are then output to a digital to analog converter block 500, which converts the digital signals to analog signals. Finally, the analog signals are output to a buffer 600, which is a unity voltage gain current amplifier. The buffer 600 accepts video signals as input, and outputs signals of the same voltage and a higher current driving capacity. Finally, the signals output from the buffer 600 are input into a switching block 700, which reorders the video signals. The outputs from the switching block are used to drive the channels of the liquid crystal device. Thus, Jeong is also silent regarding a memory used to sample and store data signals received from the latches, as recited in the claims of the present application. Accordingly, Go and Jeong, even if combined, do not disclose or suggest the features of the present invention. Withdrawal of the rejection of claim 9 is respectfully requested.

Regarding claim 10, applicant traverses the rejection because Go and Jeong, whether taken alone or in combination, do not disclose or suggest a selection signal which is used as the basis for selecting a first or second clock signal.

The examiner acknowledges that Go fails to disclose this feature, and instead relies on Jeong to disclose a selection signal. Jeong discloses a multiplexer that receives as inputs the output of a video latch for odd channel video signals and the output of a video latch for even channel video signals. There is an internal polarity control signal that is used

to select between even and odd input terminals of a multiplexer. However, the internal polarity control is not used to select a first or second clock signal, as in the present invention. Accordingly, neither of the cited references, taken alone or in combination, discloses or suggests selecting a first or second clock signal based on a selection signal. For this reason, withdrawal of the rejection of claim 10 is respectfully requested.

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Ogata et al. (JP Patent No. 407329337). Applicant traverses this rejection because the cited references do not disclose or suggest that a dot consists of a plurality of bits. Applicant further traverses the rejection because the cited prior art, taken alone or in combination, does not disclose or suggest that the output pin for a bit of a color of an odd-number dot is adjacent to an output pin of the same bit of the same color of an even-number dot.

The present specification discloses, at page 20, lines 16-23, that a dot is made up of three colors, and that each of those colors is specified using 8 bits (numbered 0-7). The bits are identified according to color, number, and whether the dot is odd or even. For example, R1E refers to the second bit that specifies the red color of an even-numbered dot; G6O refers to the seventh bit that specifies the green color of an odd-numbered dot. As shown in Fig. 15, the output pins for these bits are arranged so that, for example the output pin for bit R1O is adjacent to the output pin for bit R1E, the output pin for bit G0O is adjacent to the output pin for bit G0E, etc. Thus, the output pins are arranged so that the

output pin for a data signal of an odd-number bit of each color of each dot is adjacent to the same bit of the same color of an even-number dot.

The examiner recognizes that Go does not disclose this feature, but asserts that Ogata discloses that a dot consists of a plurality of bits. However, Ogata does not disclose this feature. Ogata discloses that each single bit corresponds to a dot in the present application. Accordingly, Ogata fails to disclose that each dot consists of a plurality of bits.

Further, Ogata shows, in Fig. 1, that the output pins for an odd-numbered bit (e.g., bit 1) are adjacent to an output pin for another odd-numbered bit (in this case, bit 3), and not an output pin for a corresponding even-numbered bit. Thus, Go and Ogata, whether taken alone or in combination, do not disclose or suggest that a dot consists of a plurality of bits, or that the output pin for a bit of a color of an odd-number dot is adjacent to an output pin of the same bit of the same color of an even-number dot. For these reasons, applicant requests withdrawal of the rejection of claim 12.

Claims 2-4 and 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Go and Misawa in view of one of Toyoshima et al. (U.S. Patent No. 6,795,049), Drake et al. (U.S. Patent No. 6,339,413), and Ogata et al. (JP Patent No. 407329337). Claims 2-4 and 6 ultimately depend from independent claim 1, and therefore include all the features of claim 1, plus additional features. Accordingly, applicant respectfully requests that the rejections of claims 2-4 and 6 be withdrawn for the reasons recited above with respect to claim 1, and because Toyoshima, Drake, and Ogata do not remedy the deficiencies identified with respect to the rejection of claim 1.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Go and Jeon, in view of Ogata. Claim 8 depends from claim 7, and therefore must incorporate all of the limitations of claim 7. Thus, applicant respectfully requests that the rejection of claim 8 be withdrawn in light of the above remarks directed to claim 7, and because Ogata does not remedy the deficiencies of identified above with respect to claim 7.

For the foregoing reasons, applicant believes that this case is in condition for allowance, which is respectfully requested. The examiner should call applicant's attorney if an interview would expedite prosecution.

Respectfully submitted,

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